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2 MOS Design from Weak through Strong Inversion. 2.1 Introduction. 2.2 MOS Design Complexity Compared to Bipolar Design. 2.3 Bipolar Transistor Collector Current and Transconductance. 2.4 MOS Drain Current and Transconductance. 2.5 MOS Drain-Source Conductance.

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Tradeoffs and Optimization in Analog CMOS Design

Tradeoffs and Optimization in Analog CMOS Design. Abstract: The selection of drain current, inversion coefficient, and channel length for each MOS device in an analog circuit results in significant tradeoffs in performance. The selection of inversion coefficient, which is a numerical measure of MOS inversion, enables design freely in weak, moderate, and strong inversion and facilitates optimum design.

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Tradeoffs and Optimization in Analog CMOS Design

Tradeoffs and optimization in analog CMOS design. Binkley, David M. John Wiley & Sons 2008 594 pages \$130.00 Hardcover TK7871 What are difficulties are in fact opportunities, an axiom certainly proved in the case of the design of analog complementary metal-oxide semiconductor (CMOS) integrated circuits.

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This book details the significant performance tradeoffs available in analog CMOS design and guides the designer towards optimum design by describing:An interpretation of MOS modeling for the analog designer, motivated by the EKV MOS model, using tabulated hand expressions and figures that give performance and tradeoffs for the design choices of drain current, inversion coefficient, and channel length; performance includes effective gate-source bias and drain-source saturation voltages ...

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